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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,484	07/21/2003	Michael Setton	015290-755	4980

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Peter K. Skiff
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,484	SETTON, MICHAEL	
	Examiner	Art Unit	
	Ron E. Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-47 and 49-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40-43* is/are allowed.

6)☒ Claim(s) *38-39, 44-47 and 49-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 38-39 and 44-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester (US 5,200,352) in view of Wu (5,880,508) in further view of admitted prior art or Ohiwa et al. (4,947,081) in further view of Shinriki et al. (US 5,292,673).

Pfiester discloses the limitations of:

forming an interfacial layer (14, fig. 1A), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate; and

forming a gate electrode of an electrically conductive material on the interfacial layer;

source and drain regions (32, fig. 1E) that are adjacent the gate electrode(col. 2, ln. 48 – col. 4, ln. 33); and

forming spacer (20, fig. 1A) adjacent to the gate electrode and on an upper surface of the interfacial layer (col. 5, lns. 30-41).

3. Pfiester reads on the claims as applied above, but does not disclose the claimed limitation(s) below of:

forming a high dielectric constant layer (8, fig. 1) on the interfacial layer;

forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides and nitrides over the entire surface of the device and then anisotropic etching the film;

forming a high dielectric constant layer (2, fig. 5a) on the interfacial layer, the comprises a material that is selected from the group consisting of Ta_2O_5, Ta2 $(O_{1-x}\ N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_t$ - $(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1 , and a solid solution of $(Ta_20_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1 and a solid solution $(Ta_2O_5)_s$-$(Al_20_3)_{1-s}$ wherein s ranges from 0.9 to less than 1 wherein the interfacial layer separates the high dielectric constant layer from the substrate;;

having a gate width of less than 0.3 micron covering the high dielectric constant layer;

wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate; and

further comprising forming second spacers on the interfacial layer adjacent to the spacers formed in step (e) and to the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film..

However,

a. Wu discloses the above claimed limitations regarding:

forming a high dielectric constant layer (8, fig. 1) on the interfacial layer (6, fig. 1), the comprises a material that is selected from the group consisting of Ta_2O_5, wherein the interfacial layer comprises silicon nitride or silicon oxynitride;

wherein the interfacial layer separates the high dielectric constant layer from the substrate; and

having a gate width of less than 0.3 micron covering the high dielectric constant layer (column 1, ln. 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pfiester with Wu, because the high dielectric constant layer provides for a gate insulator layer that reduces hot carrier effect; and the gate width of less than 0.3 micron take up less wafer real estate, which means more devices can be formed on one wafer. Note: that because the spacers are formed after the gate oxide in Pfiester the spacers would also be formed on the high dielectric layer when combining Wu with Pfiester.

b. Pfiester and Wu, fail to disclose the limitations of:

wherein the high dielectric layer comprises one of the following, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

However the admitted prior art (APA), on page 6, line 24 –26, or Ohiwa , column 2, lines 45-58, discloses that a high dielectric layer can be formed of the above compositions. Also, Ohiwa discloses that tantalum oxynitride in the claimed range is art recognized equivalent to tantalum pentoxide.

Also, in applicants' specification, page 7, line 25 – page 8 , line 3, states that it is conventional for photoresist/lithography techniques to form a gate pattern that will form the line width of a gate less than 0.3 micron.

Therefore it would have been obvious to one of ordinary skill in the art to combine the admitted prior art (APA) and/or Ohiwa with Wu, because the above listed materials are art equivalent high dielectric material with Ta_2O_5 of the Wu reference.

c. Pfiester, Wu, APA and Ohiwa, fail to disclose the limitations of:

forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides and nitrides over the entire surface of the device and then anisotropic etching the film; and

further comprising forming second spacers on the interfacial layer adjacent to the spacers formed in step (e) and to the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film..

However, Shinriki does disclose forming a spacer (12, fig. 7b) adjacent to the gate electrode on an upper surface of the high dielectric layer by deposition and a second spacer (17, fig. 7b; wherein on means touching) on the interfacial layer adjacent to the spacers formed in step (e) by deposition.

Therefore it would have been obvious to one of ordinary skill in the art to combine the Pfiester, Wu, APA and Ohiwa with Shinriki because forming a layer by deposition will requires less time and processing will be quicker.

Allowable Subject Matter

4. Claims 40-43 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singly or in combination, fails to disclose the limitations of: wherein the high dielectric layer comprises one of the following compositions, a solid solution of $(Ta_2O_5)_t - (ZrO_2)_{1-t}$, and a solid solution of $(Ta_2O_5)_u - (HfO_2)_{1-u}$ wherein t and u range from about .09 to less than 1.

Response to Arguments

6. Applicant's arguments with respect to claims 38-47 and 49-55 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
AU: 2812
January 20, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER